

**Amendments to the Specification:**

Please replace the present title with the following amended title:

“BIT LINE PAD AND BORDERLESS CONTACT ON BIT LINE STUD WITH  
LOCALIZED ETCH STOP LAYER FORMED IN AN UNDERMINED REGION.”

Please replace the first paragraph on page 1 with the following amended paragraph:

The present application is related to United States Serial No. 09/699,849, entitled “Bit Line Landing Pad and Borderless Contact on Bit Line Stud with Etch Stop Layer and Manufacturing Method Thereof”, filed of even date herewith, now U.S. Patent No 6,350,649 ; and United States Serial No. 09/699,591, entitled “Bit Line Landing Pad and Borderless Contact on Bit Line Stud with Localized Etch Stop Layer and Manufacturing Method Thereof”, filed of even date herewith, now U.S. Patent No. 6,518,671 and incorporated herein by reference.

Please replace the paragraph at page 7, lines 12-18 of the Specification with the following amended paragraph:

A first etch-stop material layer 224A is selectively patterned on the upper surface of the lower-level stud 220A, and on a portion of the inter-layer dielectric 202 surrounding the lower-level stud 220A. The first etch-stop material layer 224B is further patterned on the conductive line 222. A second etch-stop material layer is patterned over the resulting structure, and selectively removed so as to provide for lateral spacers 226 on the side walls of the conductive line 222. The first and second etch-stop material layers 224A, 224B may comprise similar, or different, materials, for example  $\text{Si}_3\text{N}_4$ ,  $\text{Ta}_2\text{O}_5$  or  $\text{Al}_2\text{O}_3$ .

Please replace the paragraph at page 11, lines 7-11 with the following amended paragraph:

FIGs. 4A-4F illustrates an alternative embodiment of the present invention. In FIGs. 4A, 4B, and 4C, inter-level studs 220A, 220B are formed through second and first inter-layer dielectric layers 202, 302 and a first etch-stop layer 304 as described above with reference to FIGs. 3A-3C. An undermined region of the second dielectric layer 320[[A]] is likewise formed below the first etch-stop layer 304, as described above.